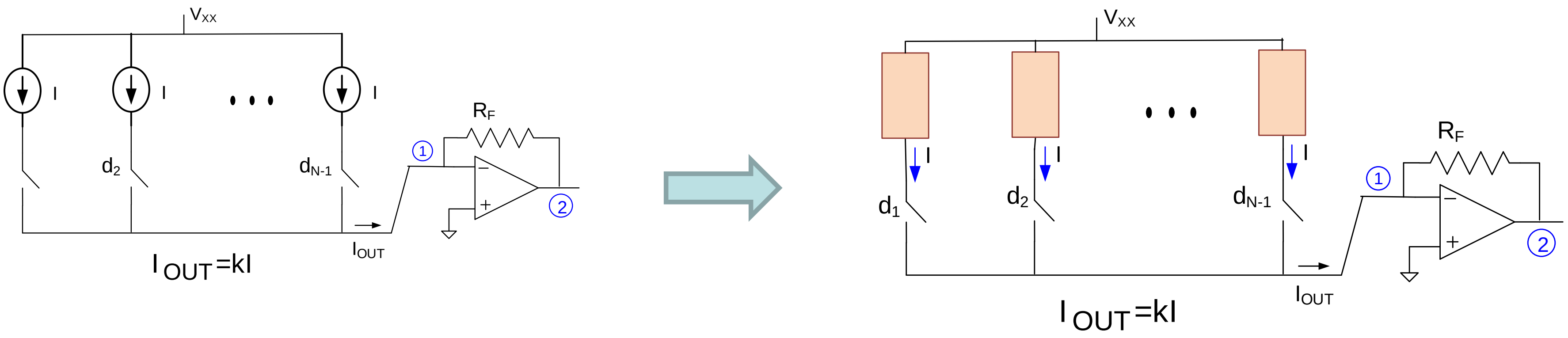
EE 435

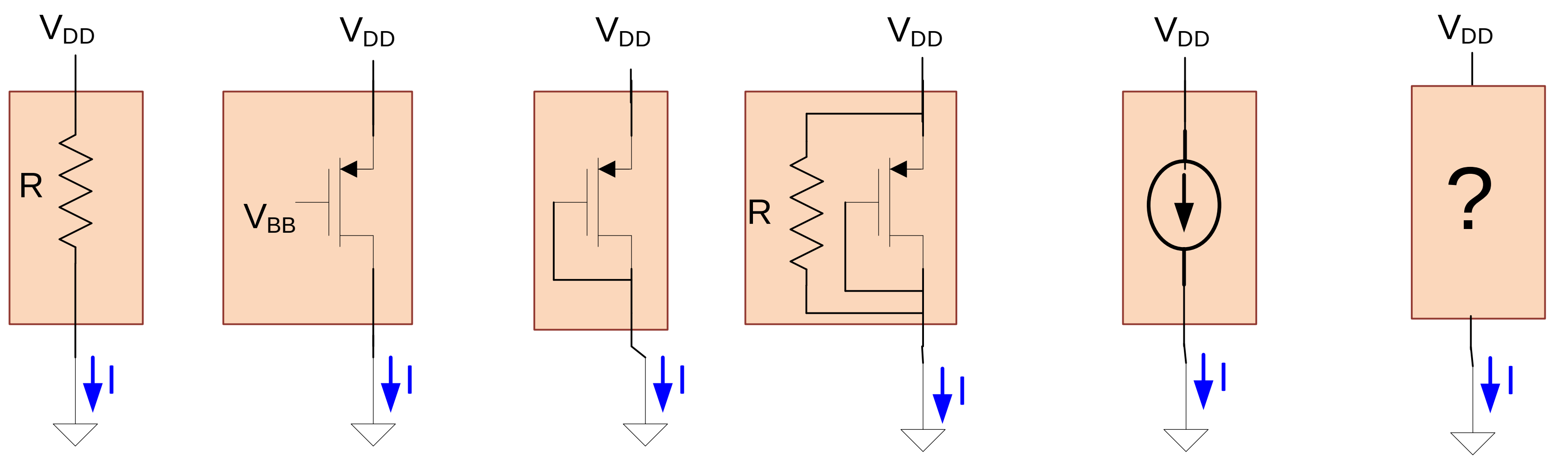
Lecture 34

- Current Steering DACs
- Charge Redistribution Circuits

Current Steering DACs



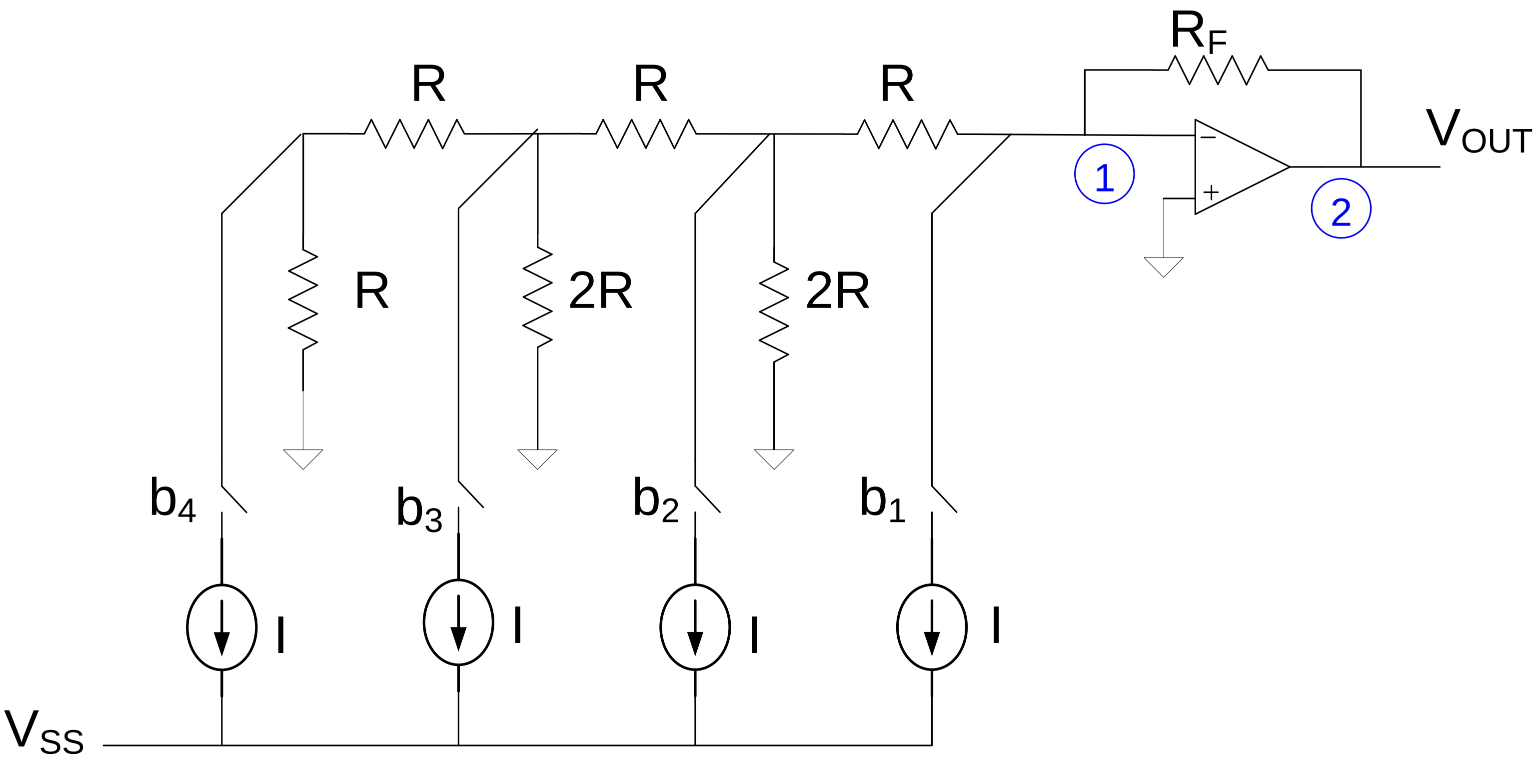
What is important is the current generated, not whether it comes from a “current source”



Many potential current generator blocks, just require that all be ideally identical

Review from Last Lecture

Another R-2R DAC



Requires matching both current sources and resistors

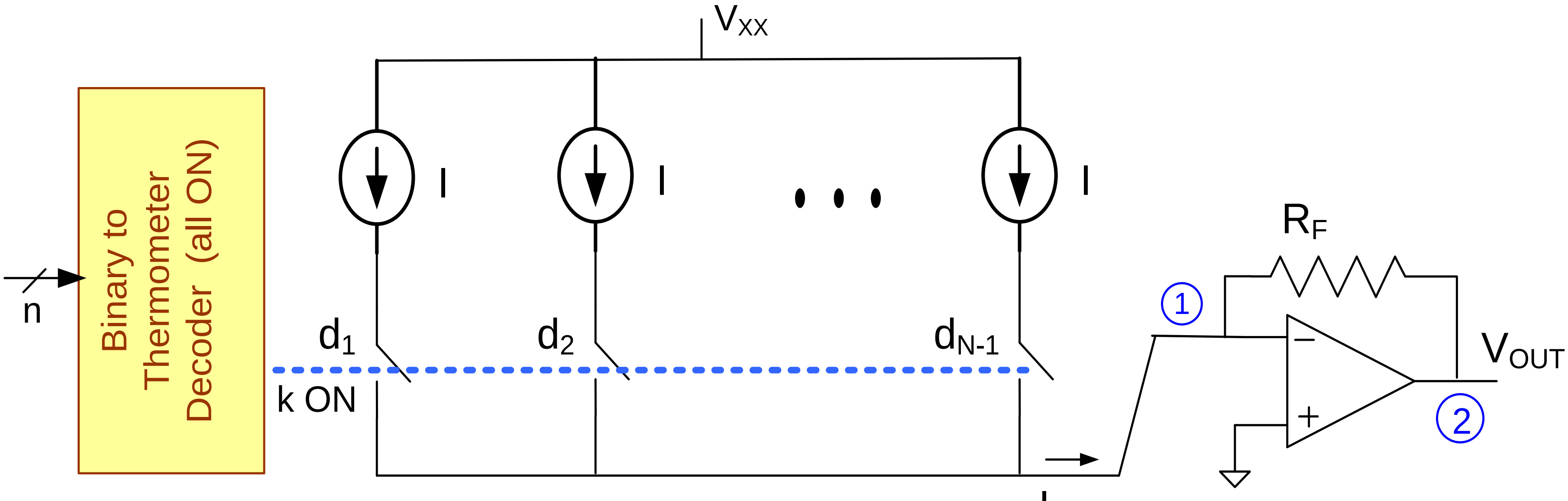
But switch impedance does not affect performance

β is independent of Boolean code

Node voltages in R/2R block must change for any input transitions

Review from Last Lecture

Current Steering DAC

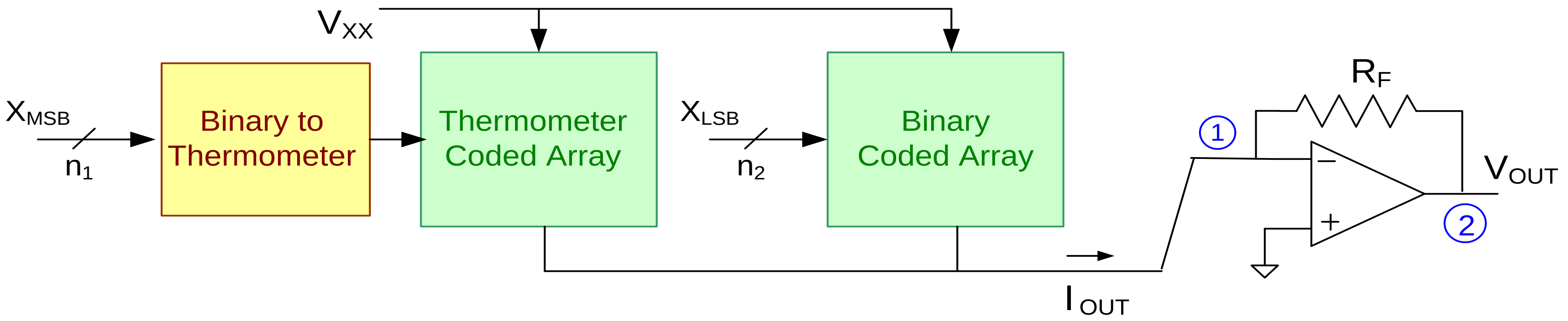


$$I_{OUT}=kI$$

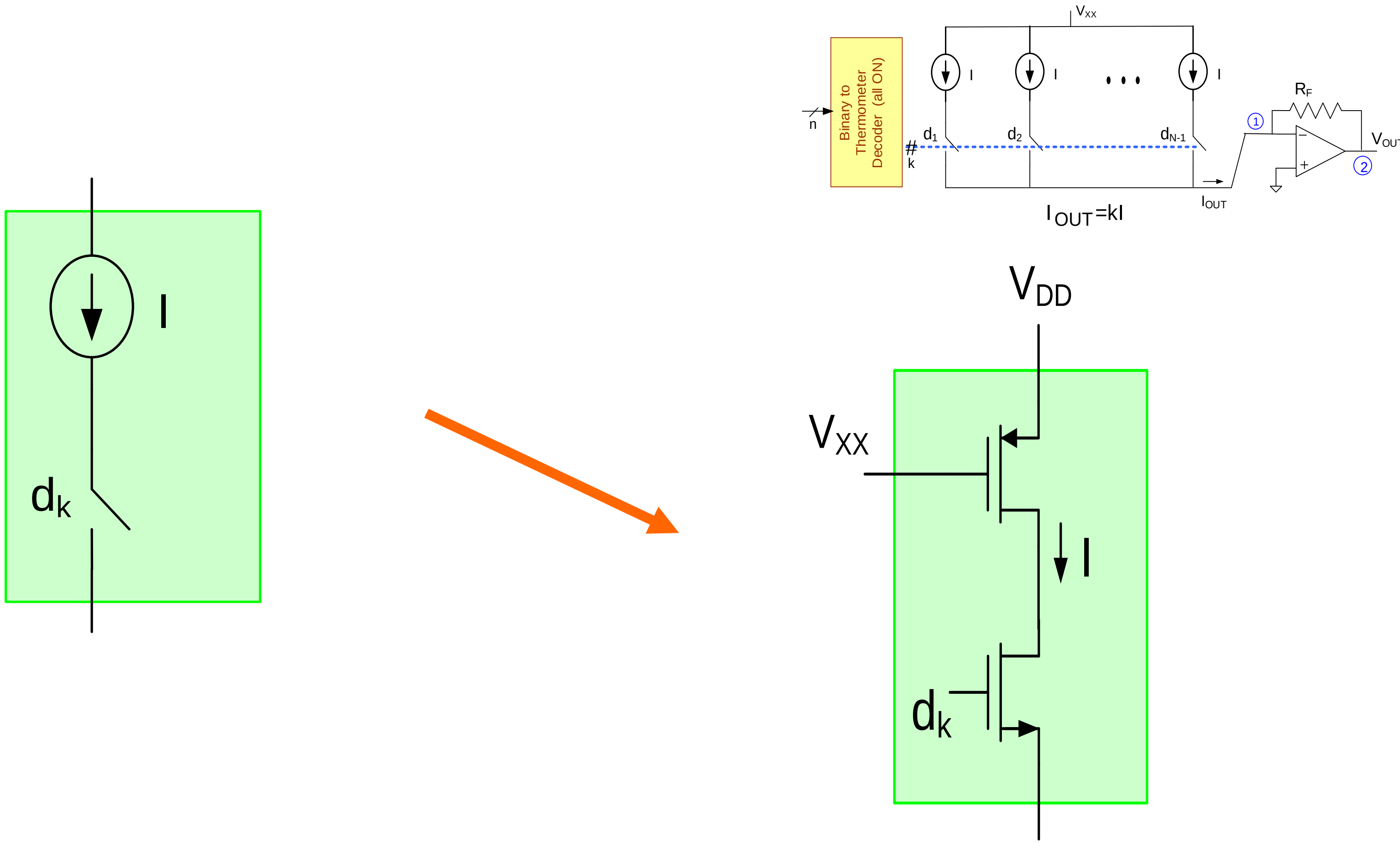
Switch impedance of little concern

Review from Last Lecture

Current Steering DAC



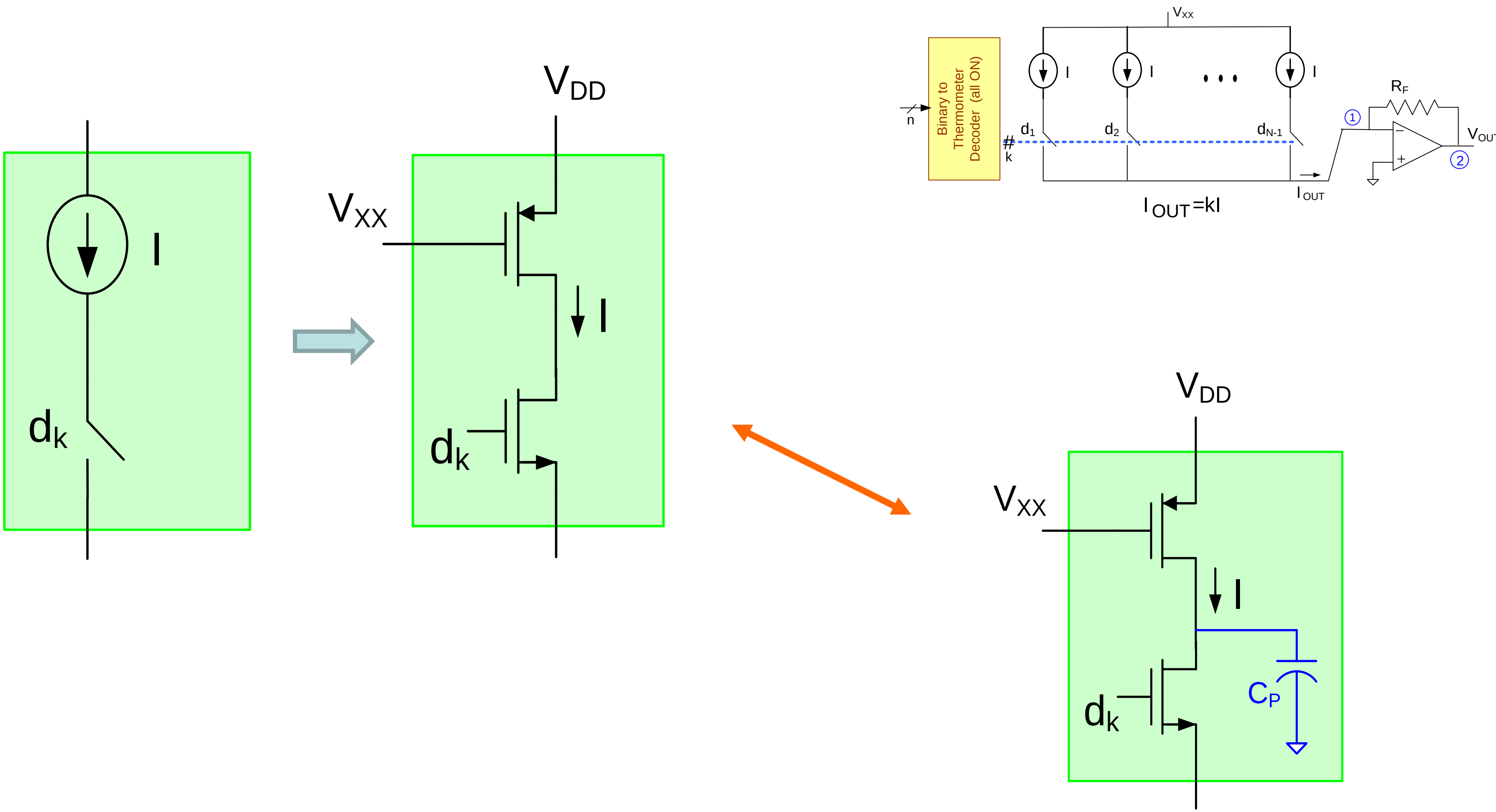
Current Steering DAC



Is linearity or output impedance of current source of concern?

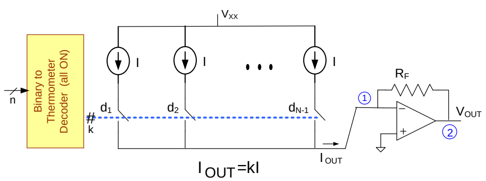
Not if individual slices are matched !

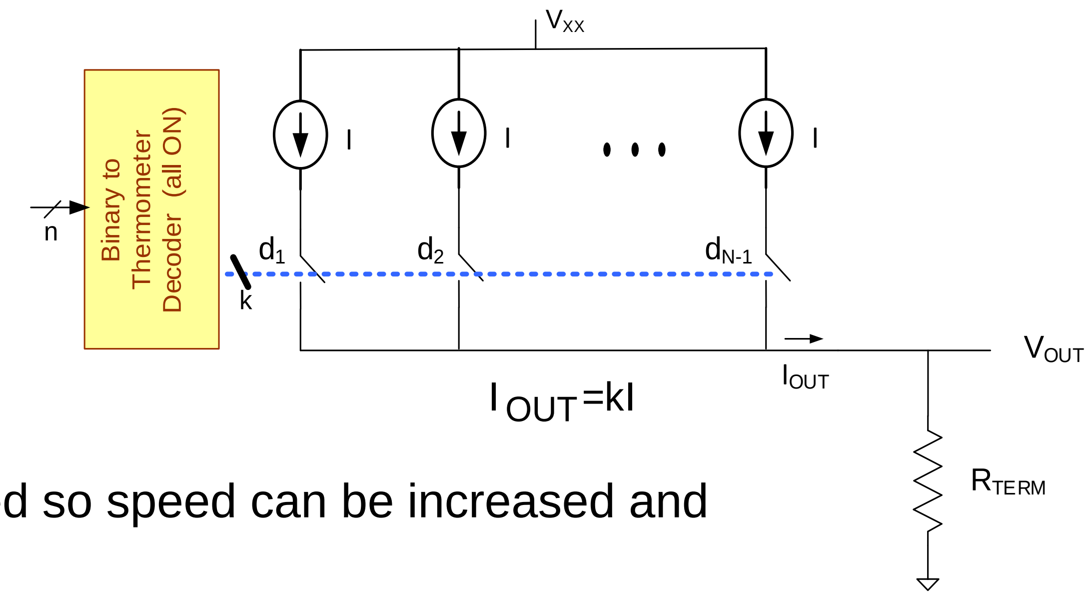
Current Steering DAC



Review from Last Lecture

Current Steering DAC





Op Amp can be eliminated so speed can be increased and power reduced

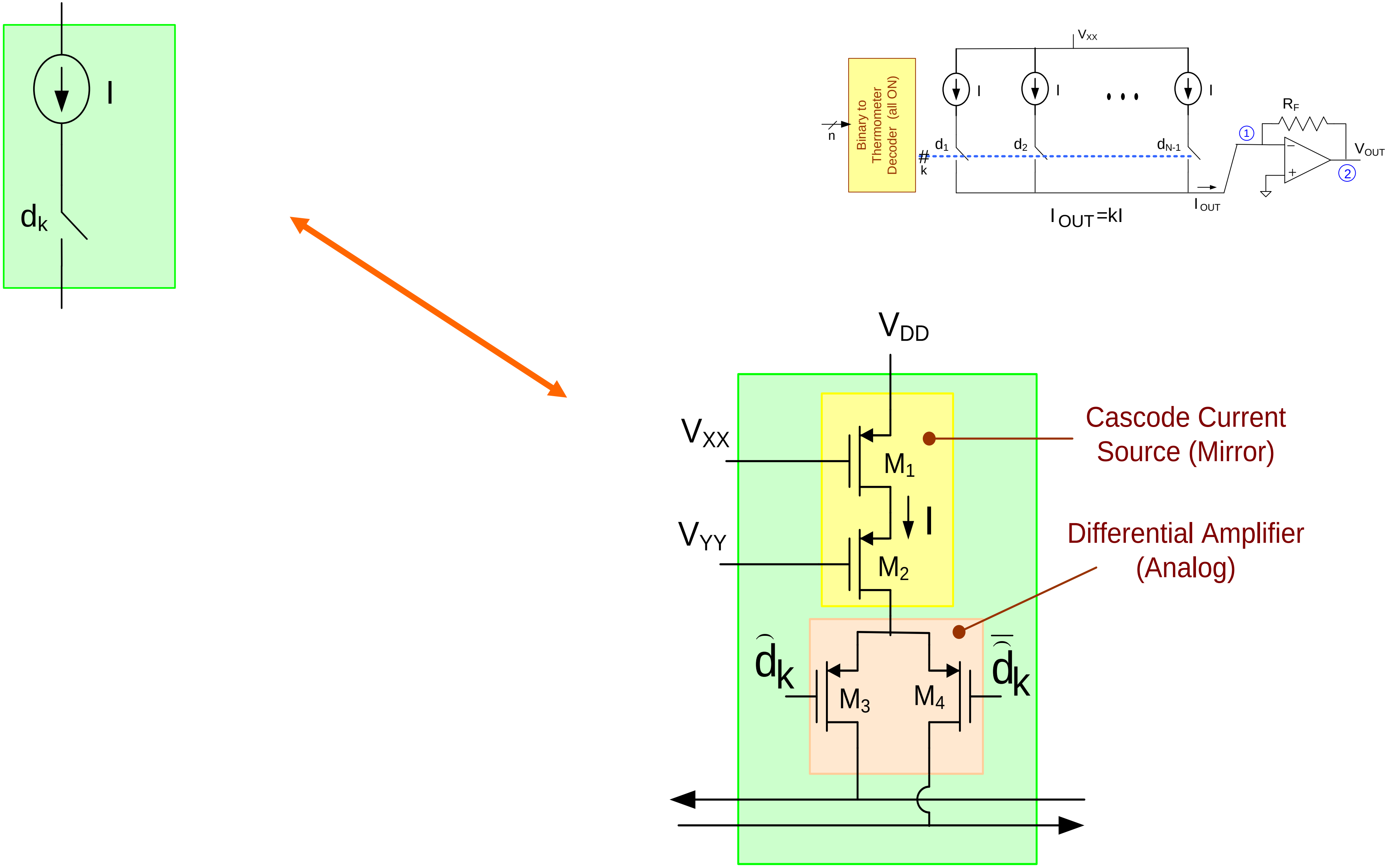
R_{TERM} often 50Ω or 100Ω

R_{TERM} can be internal or external

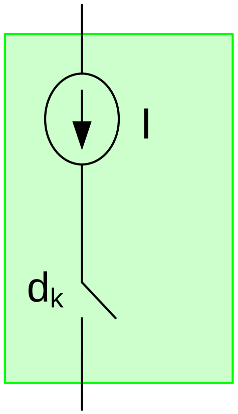
Switch impedance now of concern

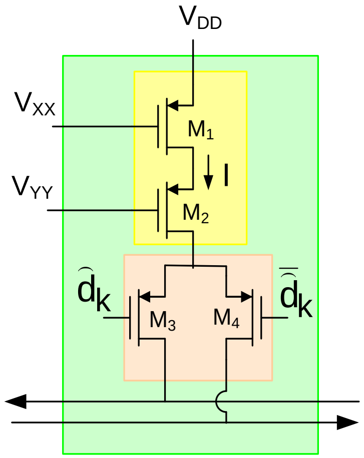
Output impedance of current sources now of concern

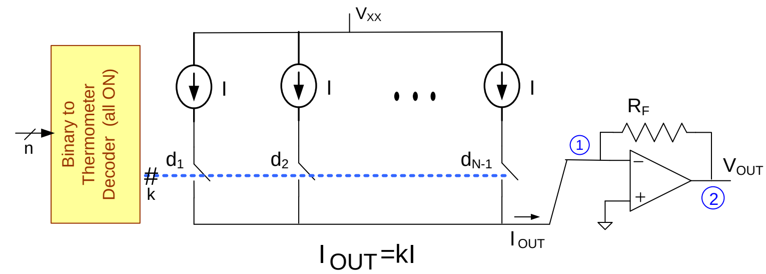
Current Steering DAC

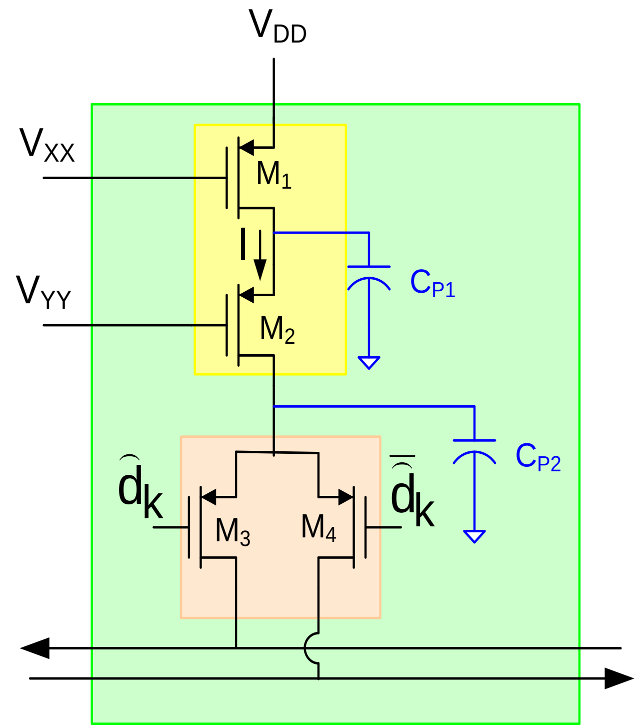


Current Steering DAC

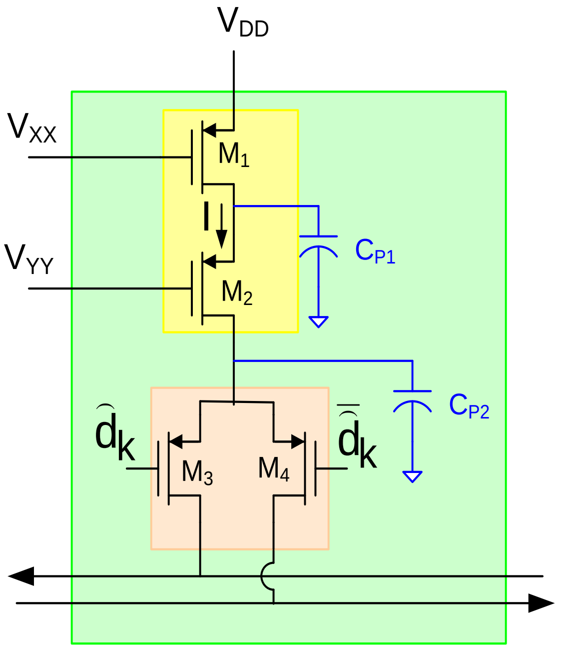


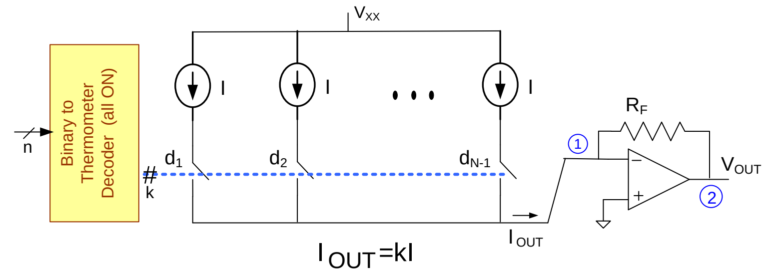


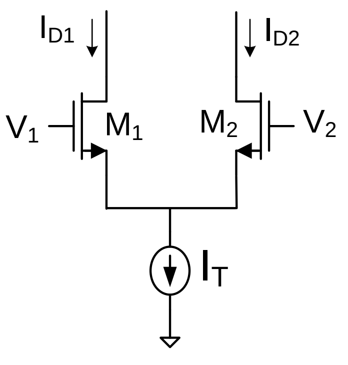


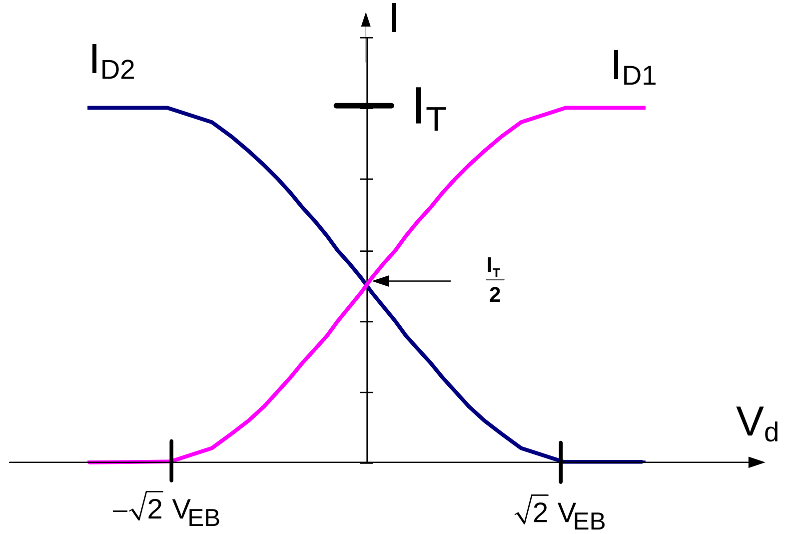


Current Steering DAC



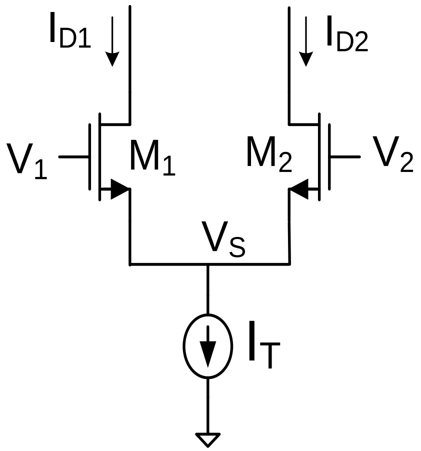


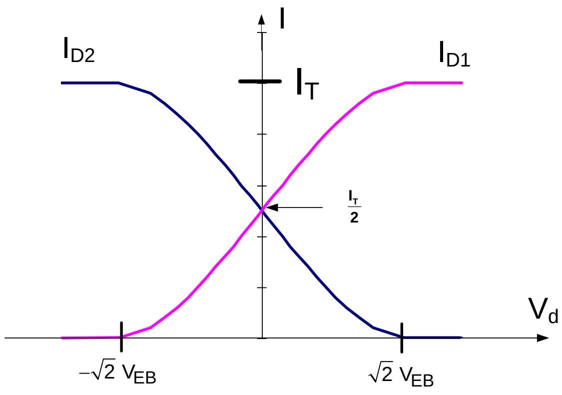




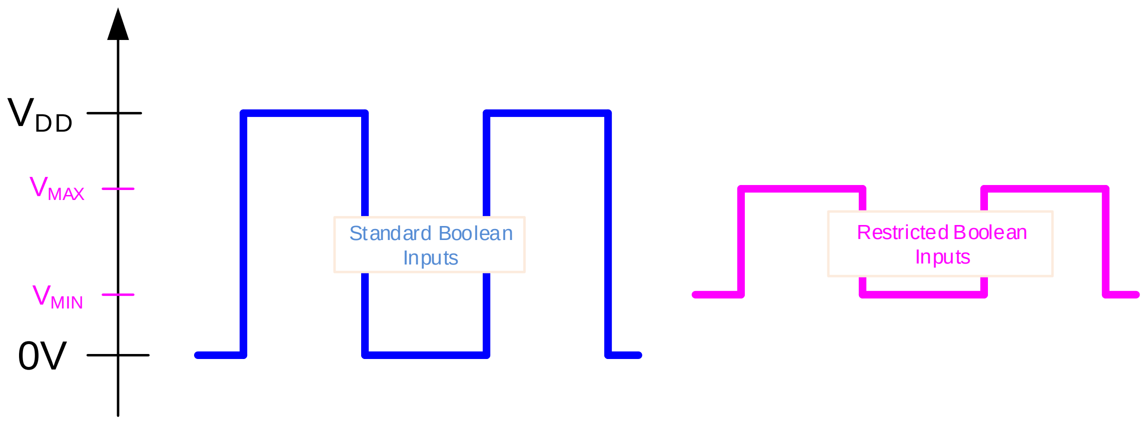
- Need only signal swing of $2\sqrt{2}V_{EB}$ to steer currents (so can reduce turn-on and turn-off times)
- Steering also results in cascoding with M_3 and M_4 thus increasing output impedance of current source (so can probably eliminate M_2)

Current Steering DAC

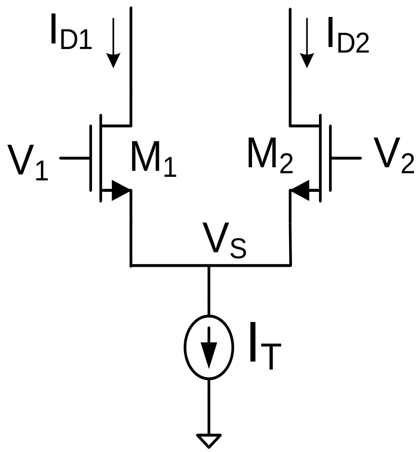


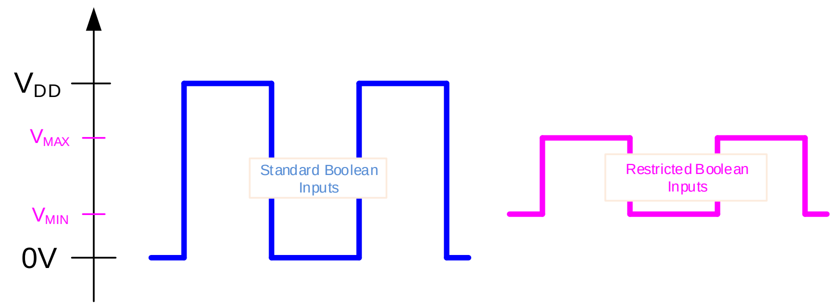


Reduced Signal Swing on V_S Node with Current Steering

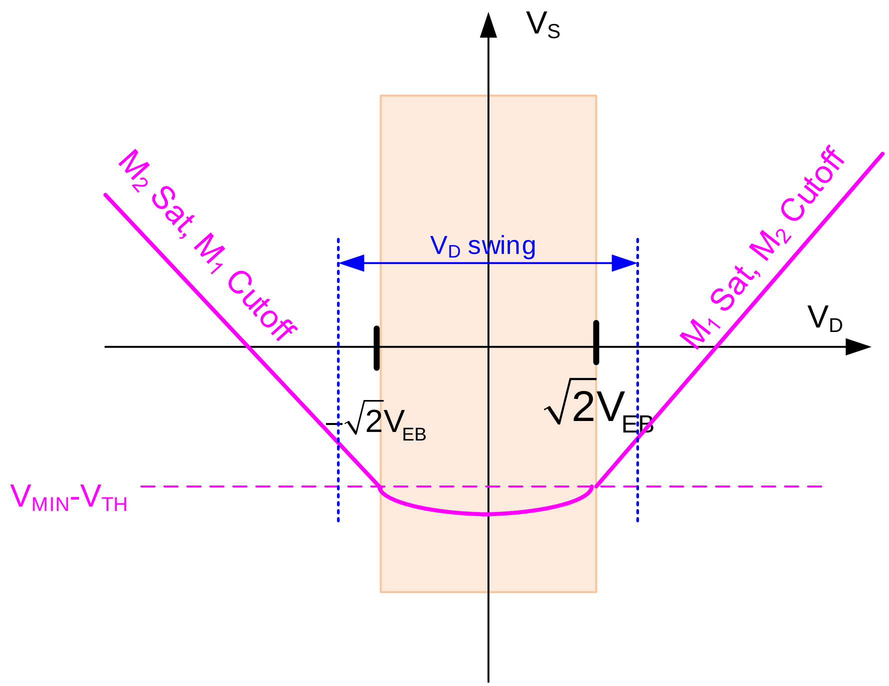


Current Steering DAC

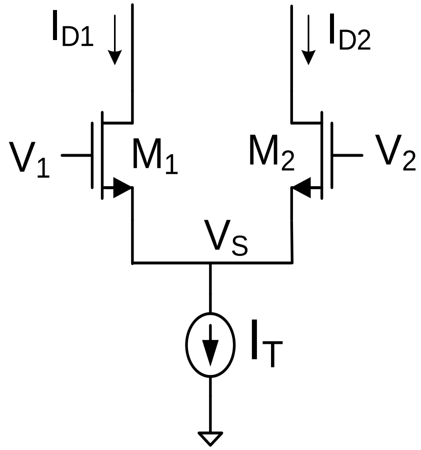


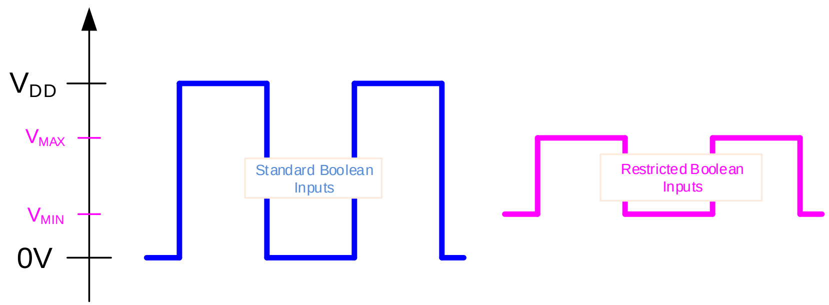


Reduced Signal Swing on V_S Node with Current Steering



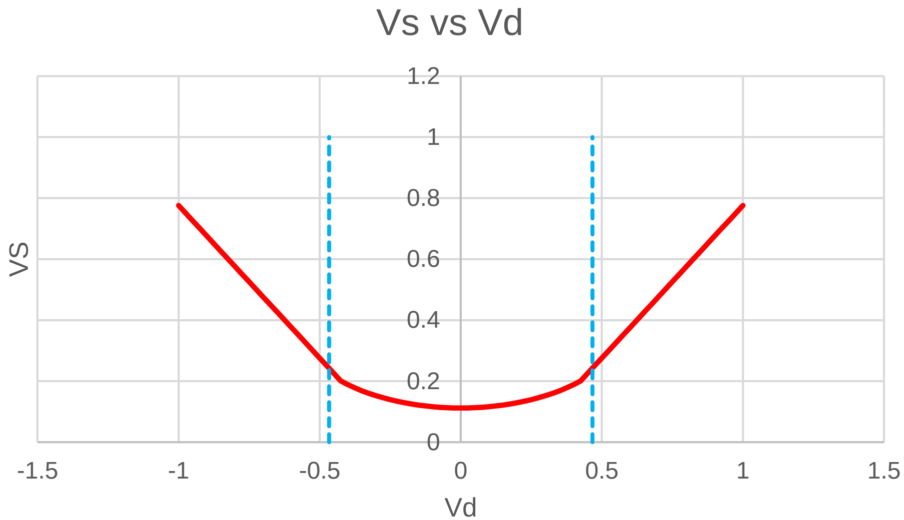
Current Steering DAC





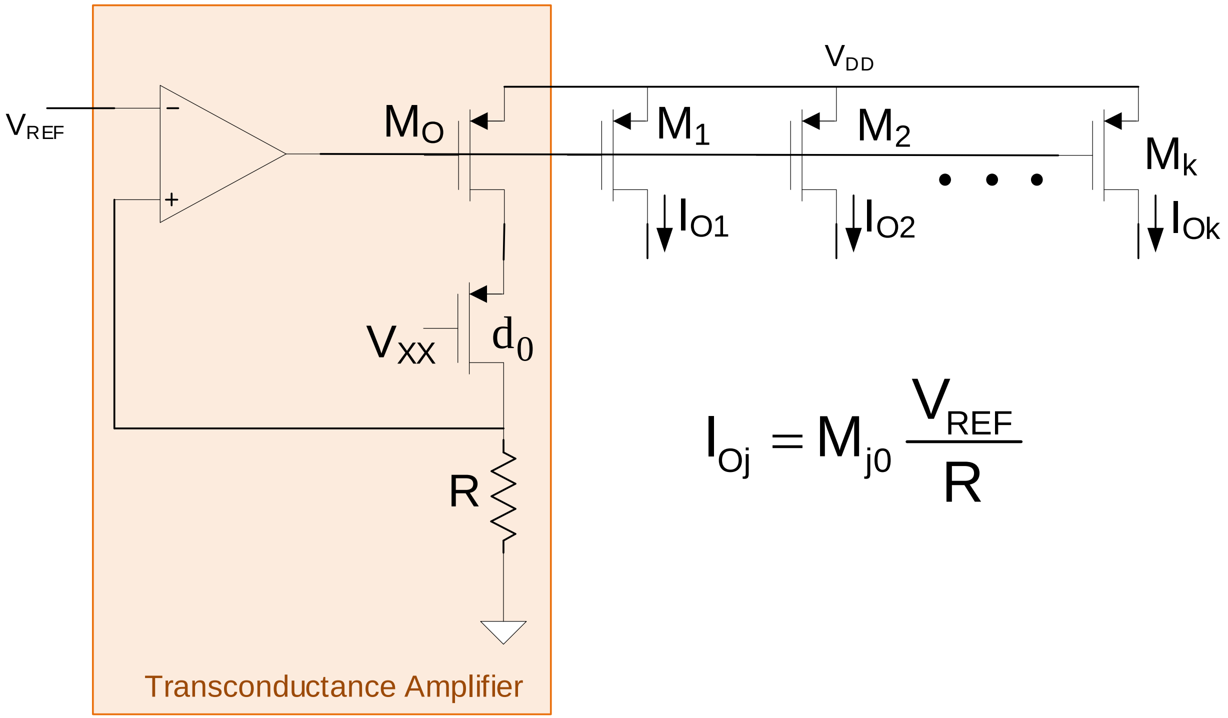
Reduced Signal Swing on V_S Node with Current Steering

Simulation Results: V_{TH}=0.4V, V_{MIN}=0.6V, V_{MAX}=1.07V,V_{EB}=0.3V,γ=1.1



V_S swing about 100mV

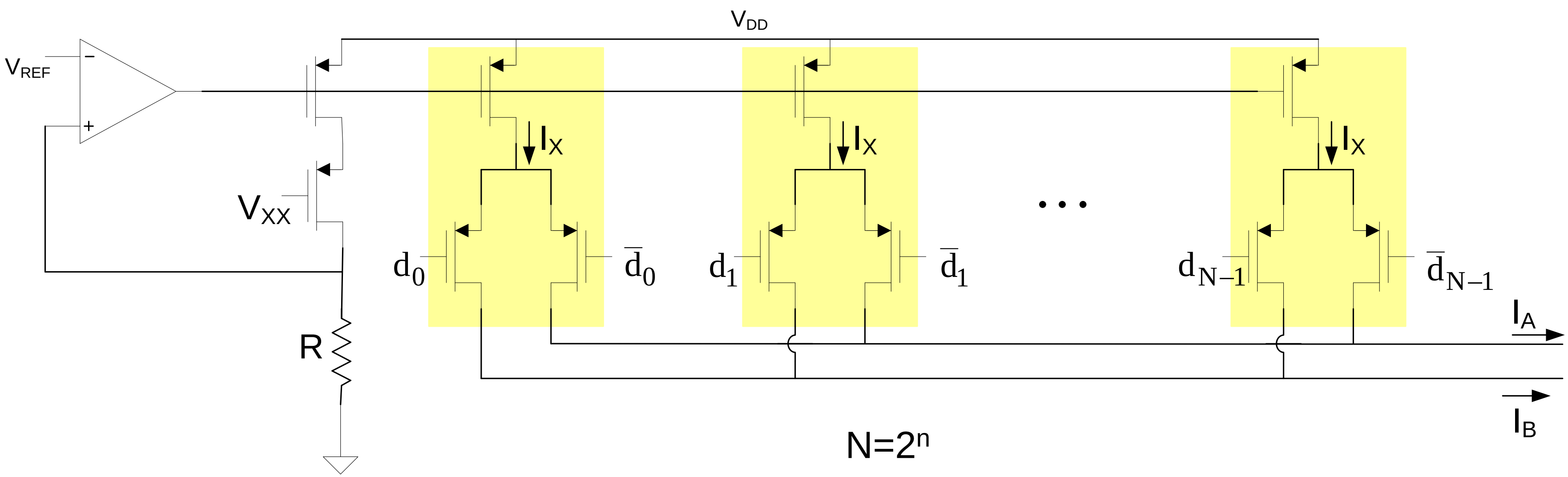
Multiple-output Transconductance Amplifier



$$I_{Oj} = M_{j0} \frac{V_{REF}}{R}$$

- Good linearity
- Each additional output requires only one additional transistor

Current Steering DAC with Supply Independent Biasing



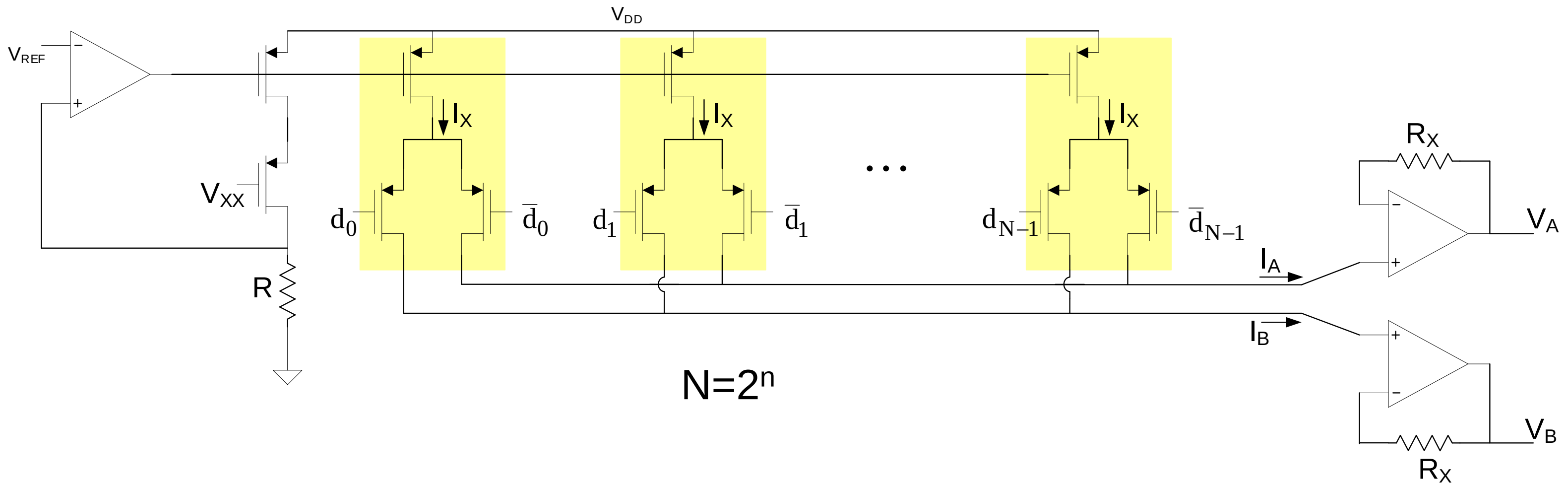
If transistors on top row are all matched, $I_X = V_{REF}/R$

Thermometer coded structure (requires binary to thermometer decoder)

$$I_A = \left(\frac{V_{REF}}{R}\right)\sum_{i=0}^{N-1} d_i$$

Provides Differential Output Currents

Current Steering DAC with Supply Independent Biasing

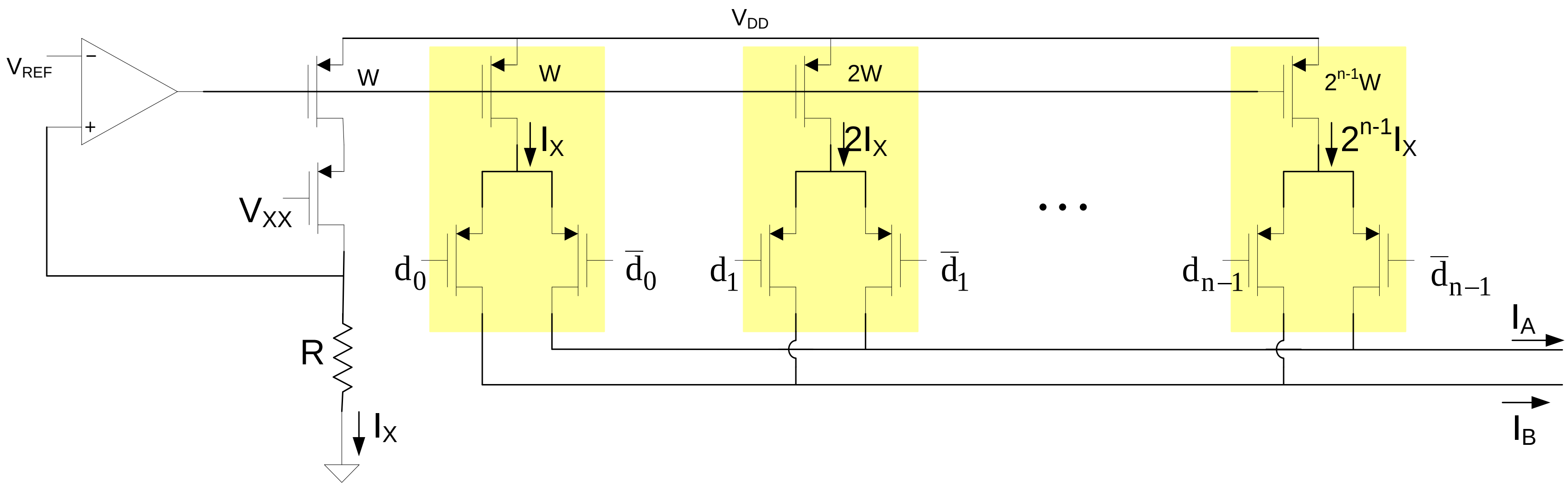


If transistors on top row are all matched, $I_X = V_{REF}/R$

$$V_A = \left(-V_{REF}\frac{R_A}{R}\right)\sum_{i=0}^{N-1} d_i$$

Provides Differential Output Voltages

Current Current Steering DAC with Supply Independent Biasing

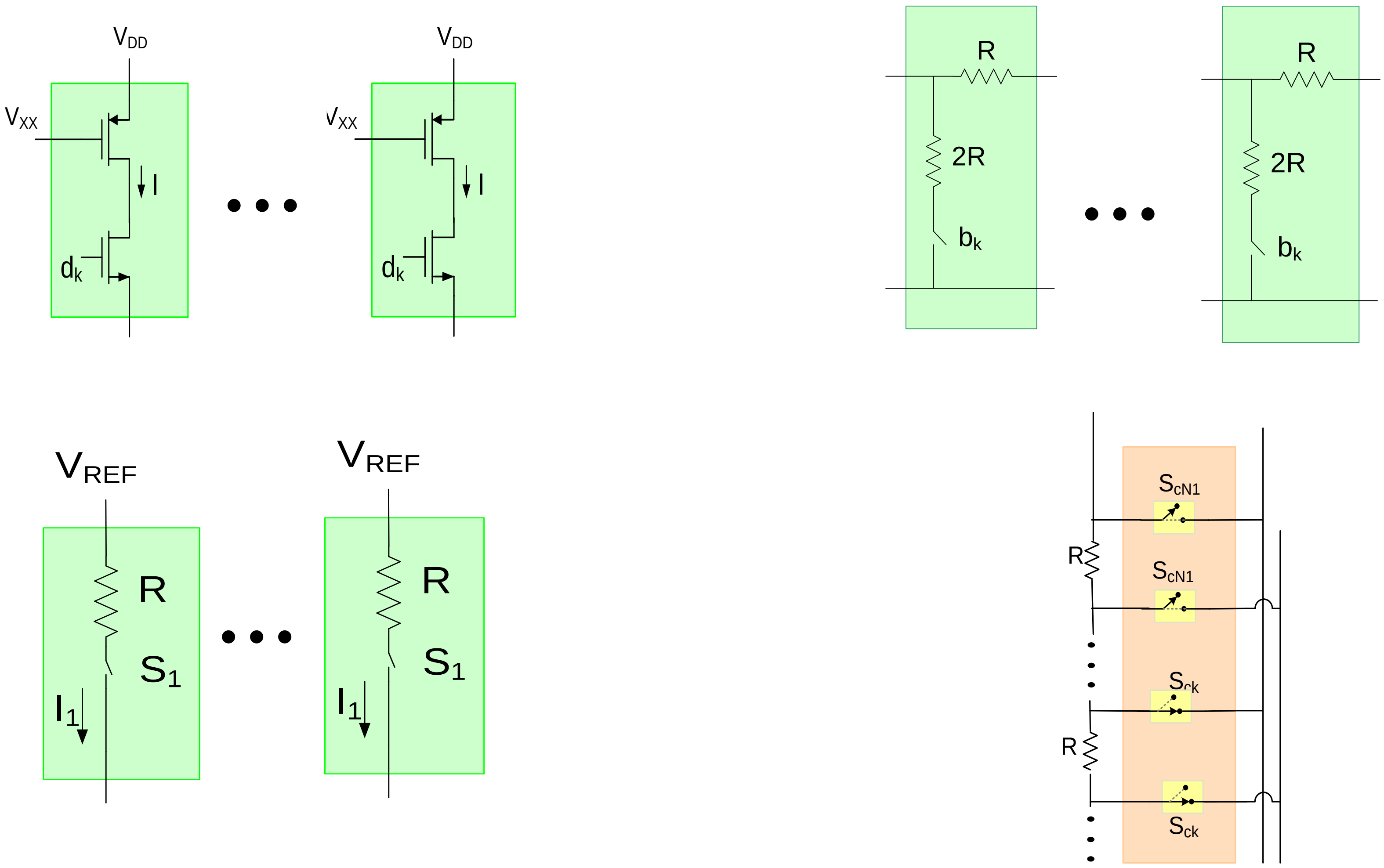


If transistors on top row are binary weighted

$$I_A = \left(\frac{V_{REF}}{R}\right) \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$

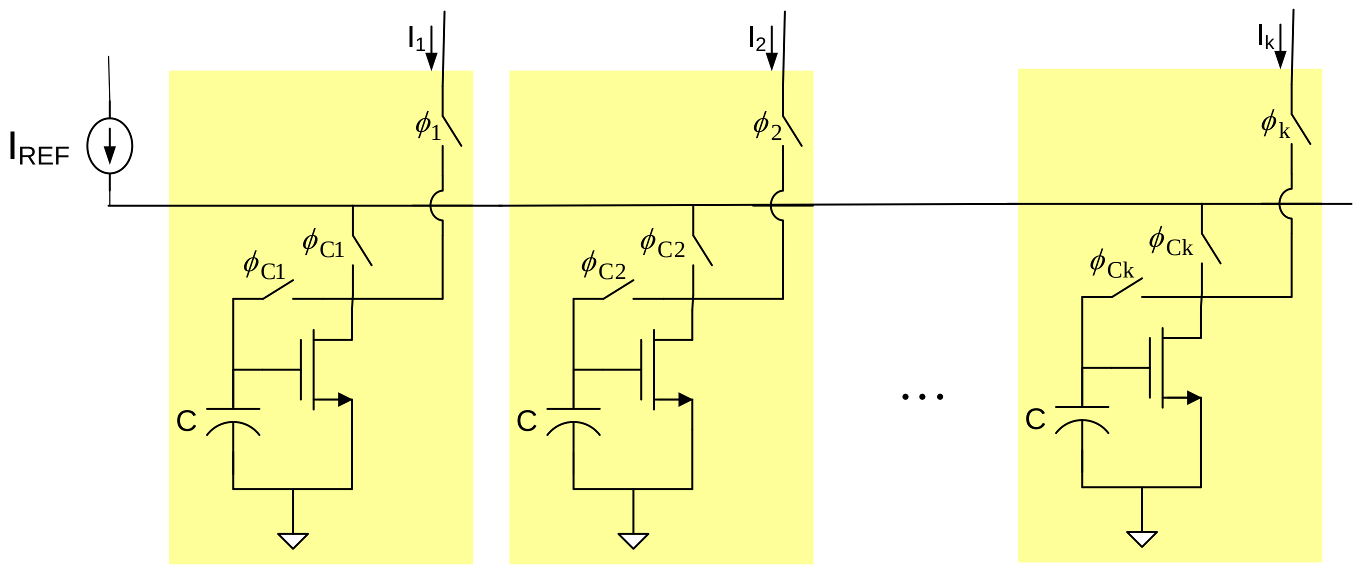
Provides Differential Output Currents

Matching is Critical in all DAC Considered



Obtaining adequate matching remains one of the major challenges facing the designer!

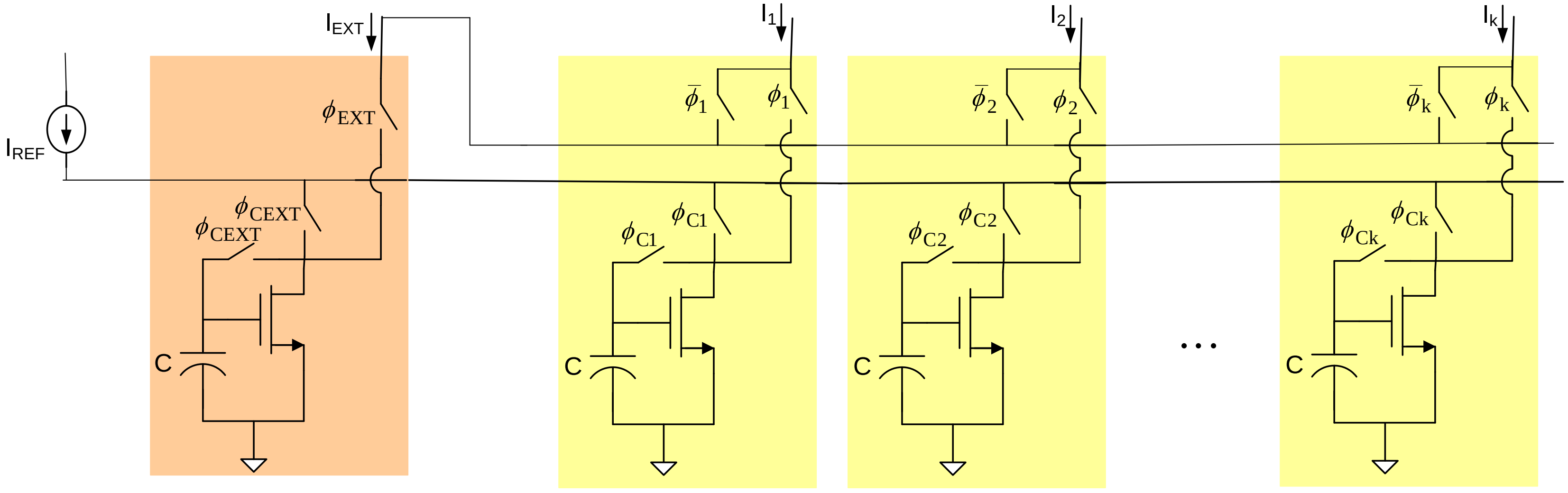
Dynamic Current Source Matching



- $\varphi_1, \ldots \varphi_k \ldots \varphi_n$ distinct from $d_1, \ldots d_n$ (not shown)
- Correct charge is stored on C to make all currents equal to I_{REF}
- Does not require matching of transistors or capacitors
- Requires refreshing to keep charge on C
- Form of self-calibration
- Calibrates current sources one at a time
- Current source unavailable for use while calibrating
- Can be directly used in DACs (thermometer of binary coded)

Often termed “Current Copier” or “Current Replication” circuit

Dynamic Current Source Matching



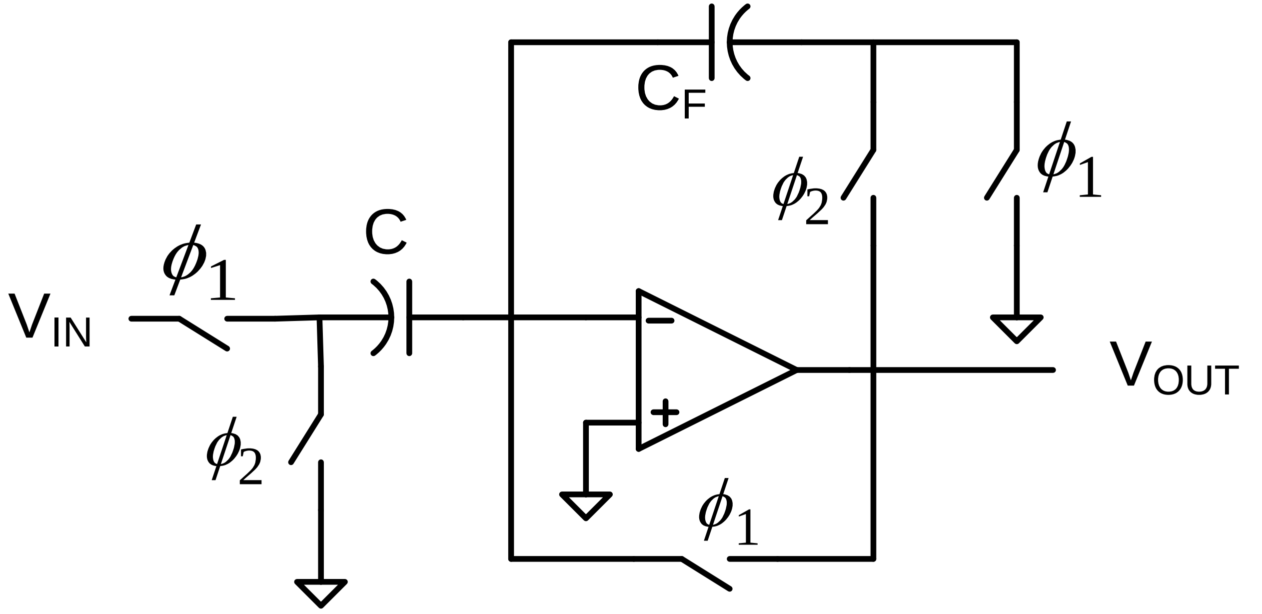
Extra current source can be added to facilitate background calibration

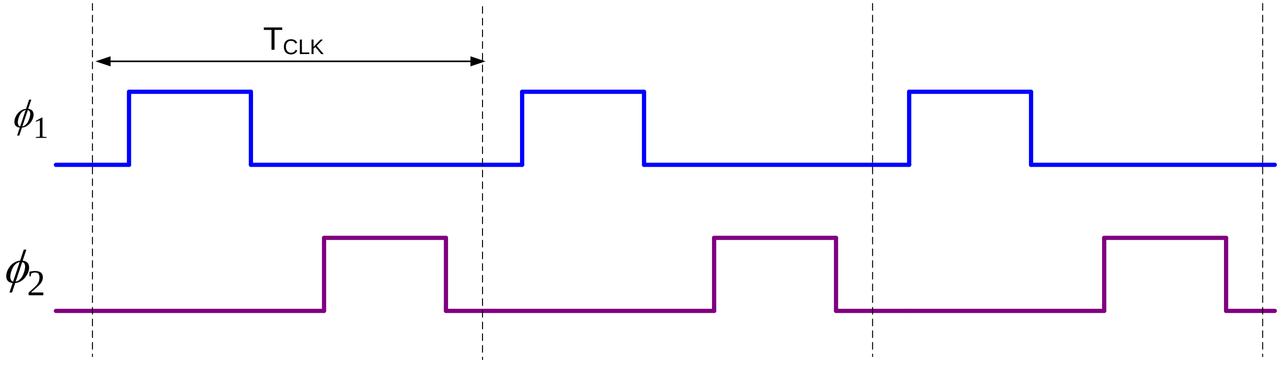
Charge Redistribution DACs

- Previous DACs based upon matching of resistors or transistors
- Switch impedance was of concern in most of the structures
- Capacitor matching can be very good in most processes and area required for a given level of matching may be smaller for capacitors than for resistors or transistors in some processes
- Capacitor linearity is often excellent

Will now focus on building DACs that take advantage of good capacitor matching and linearity

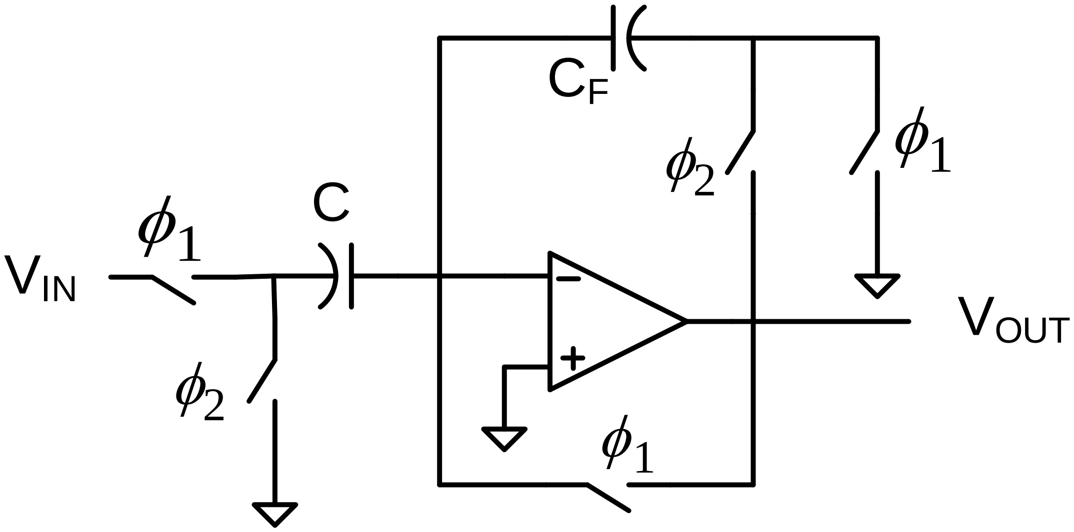
A charge redistribution circuit

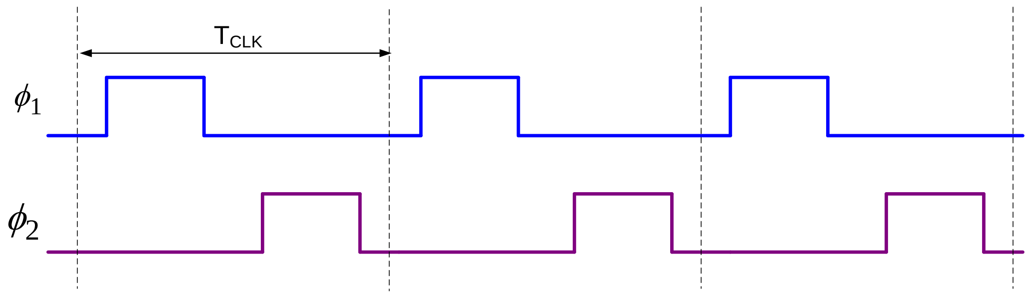




Clocks are complimentary non-overlapping

A charge redistribution circuit





During phase φ_1

$$Q_{\phi 1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase φ_2

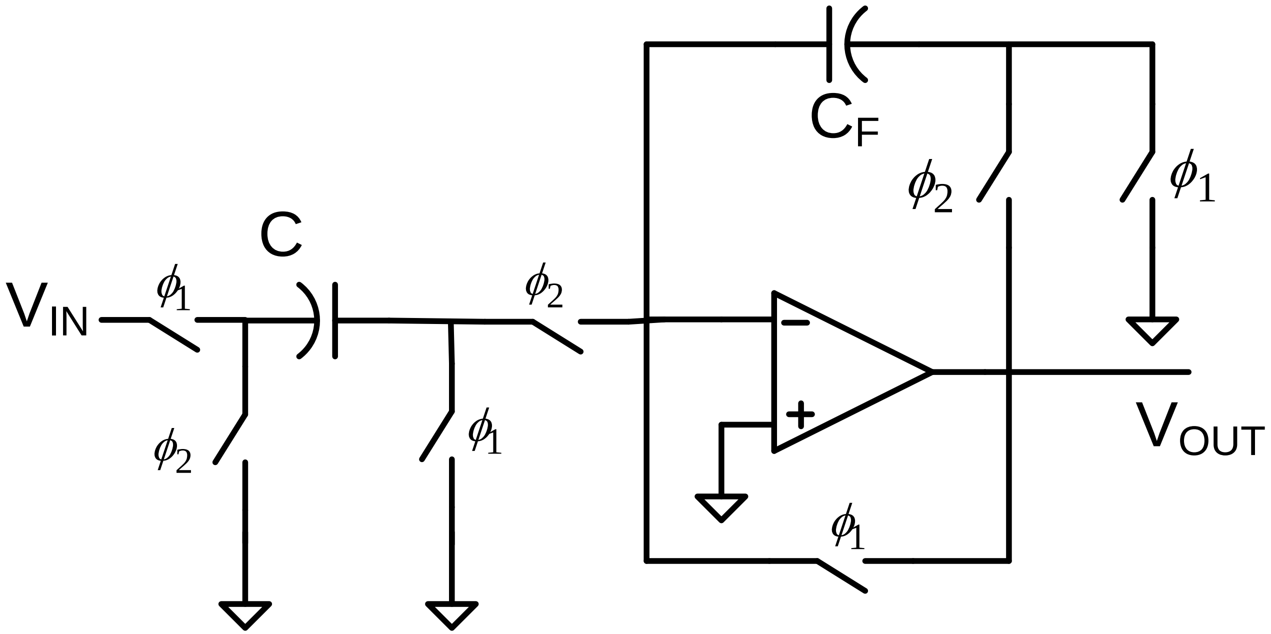
$$\frac{Q_{\phi 1}}{C_F} = V_{OUT}$$

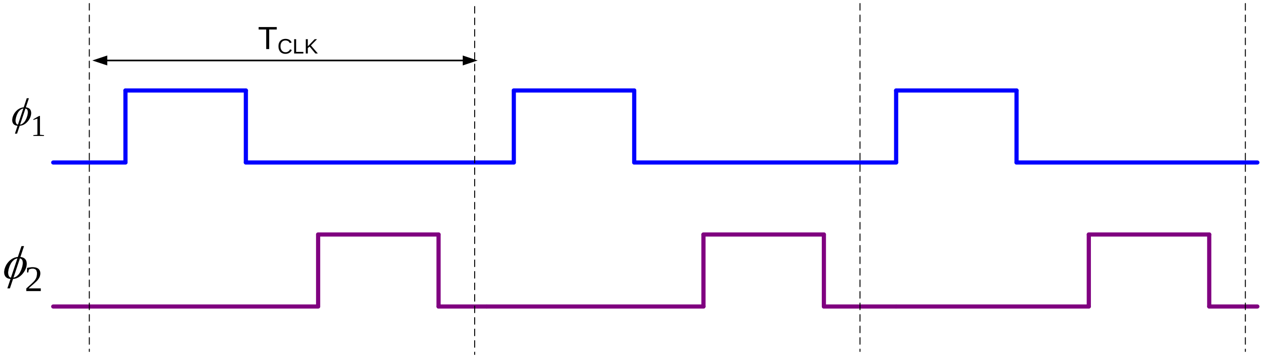
$$\frac{CV_{IN}}{C_F} = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{C}{C_F}$$

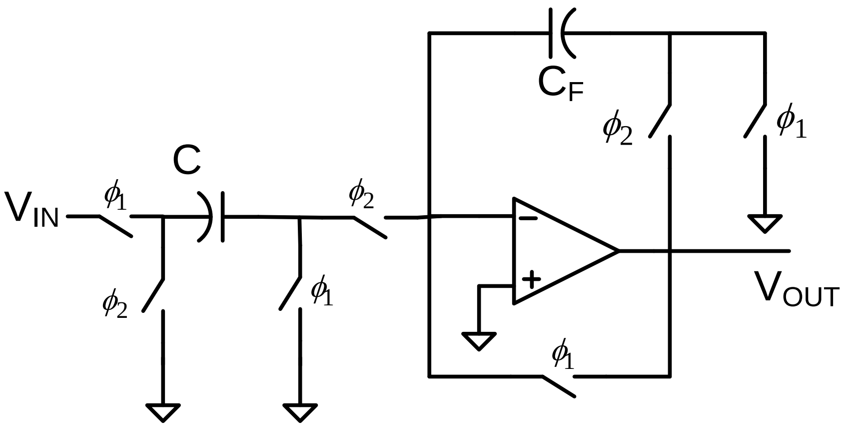
Serves as a noninverting amplifier
Gain can be very accurate
Output valid only during Φ_2

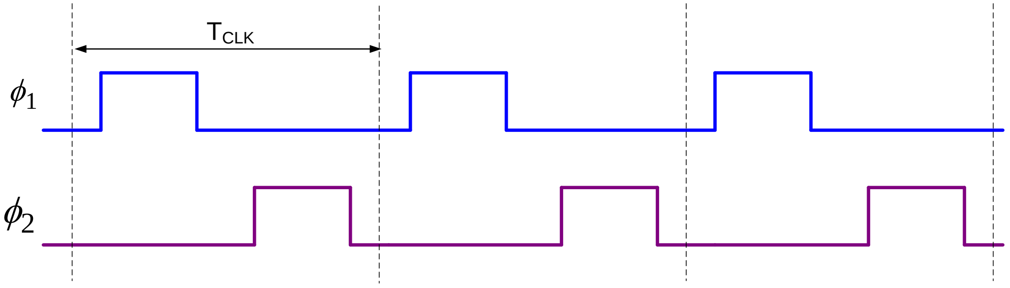
Another charge redistribution circuit





A charge redistribution circuit





During phase φ_1

$$Q_{\phi 1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase φ_2

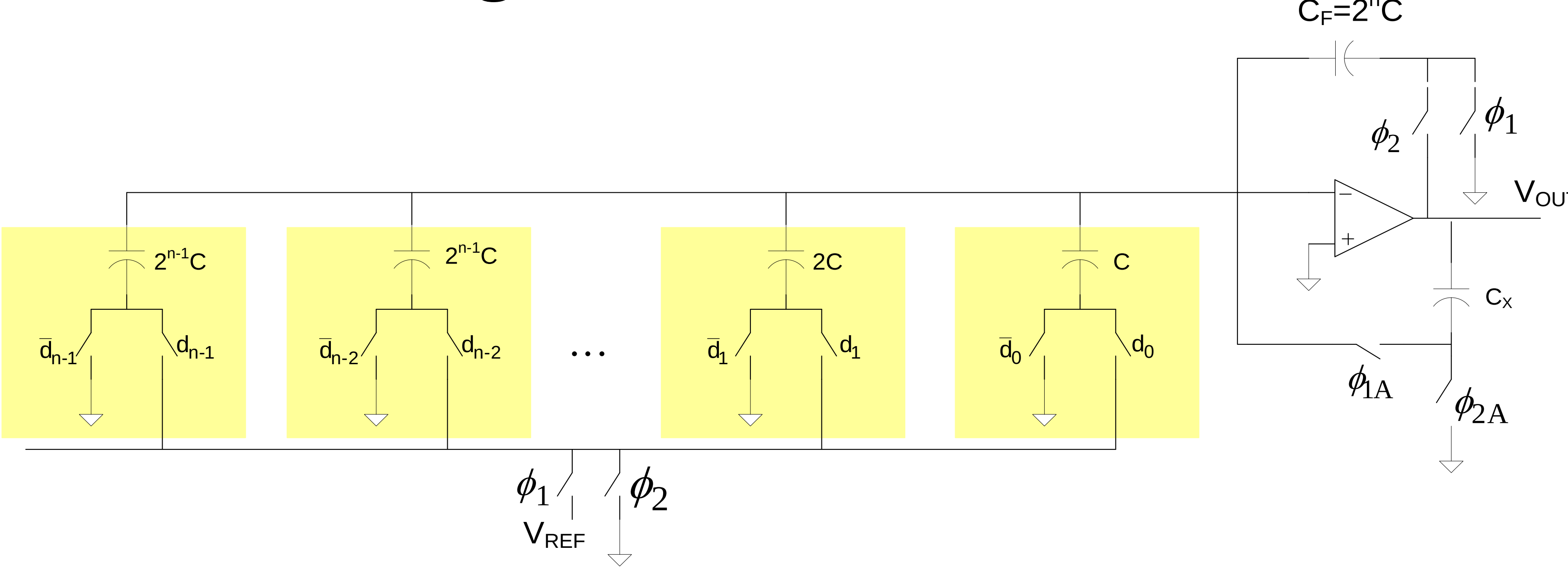
$$\frac{-Q_{\phi 1}}{C_F} = V_{OUT}$$

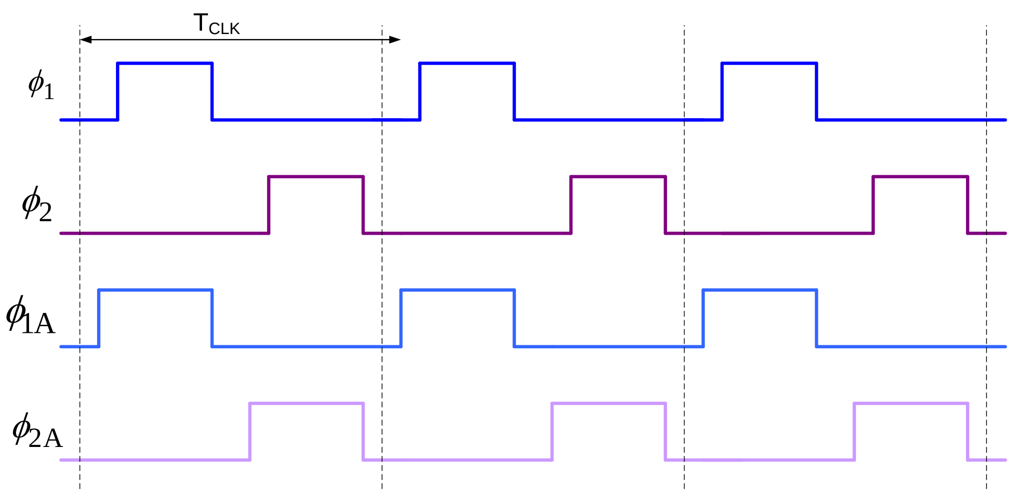
$$\frac{-CV_{IN}}{C_F} = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{C}{C_F}$$

Serves as a inverting amplifier
Gain can be very accurate
Output valid only during Φ_2

A charge redistribution DAC

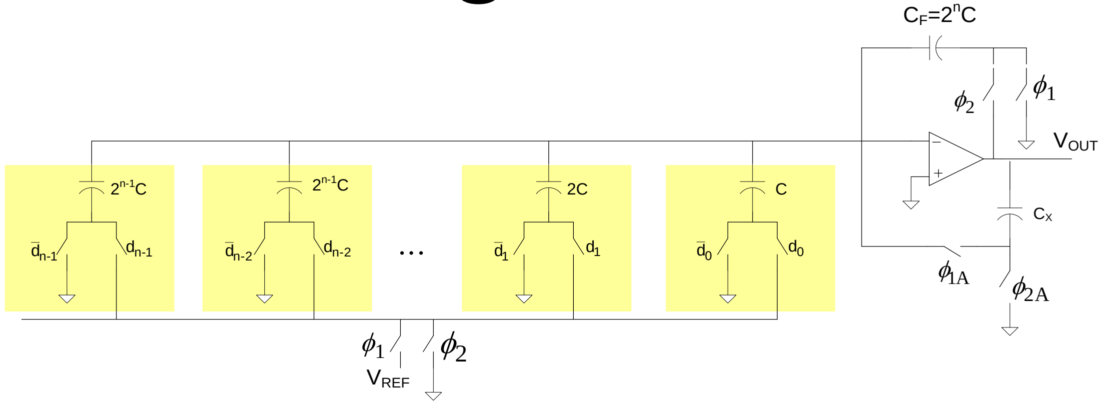


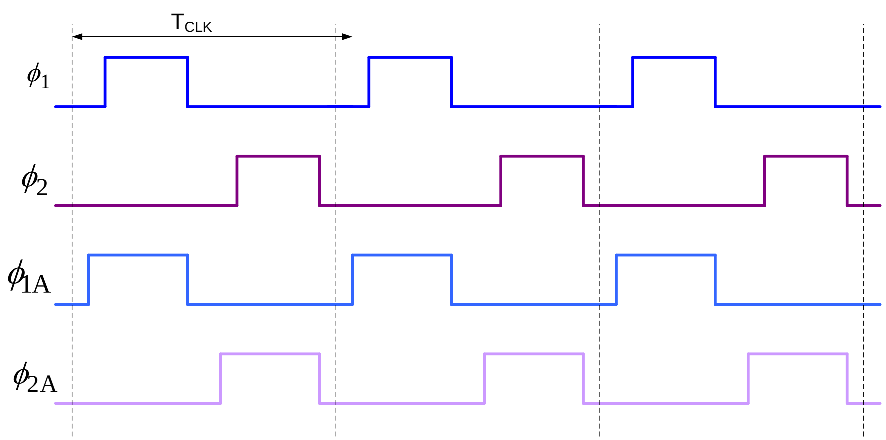


C_X does some good things
(mitigates V_{OS}, 1/f noise and finite gain errors)

Will not consider CX affects at this time

A charge redistribution DAC





During phase φ_1

$$Q_{\phi 1} = V_{REF} \sum_{i=0}^{n-1} d_i \bullet 2^i C$$

$$Q_{CF} = 0$$

During phase φ_2

$$V_{OUT}(\phi_2) = \frac{1}{C_F} Q_{\phi 1}$$

$$V_{OUT}(\phi_2) = \frac{1}{2^n C} V_{REF} \sum_{i=0}^{n-1} d_i \bullet 2^i C$$

$$V_{OUT}(\phi_2) = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$

Stay Safe and Stay Healthy !

End of Lecture 34